AMENDMENTS

Please amend the above-identified application as follows:

In the Claims:

This listing of claims replaces all prior versions and listings of claims in the application.

1. (Currently Amended) An apparatus for performing the addition of ~~a~~ propagate, kill, and generate recoded numbers, said apparatus comprising:

a circuitry configured to receive at least a first operand, ~~and~~ a second operand, and a carry-in bit, the first and second operands comprising respective first and second propagate, kill, and generate recoded number representations of respective first and second binary operands;

a first carry-save adder configured to add said first operand and said second operand to generate a third propagate, kill, and generate recoded number representation and a carry-out bit; and

a modified carry-save adder configured to receive the third propagate, kill, and generate recoded number representation from the first carry-save adder, the carry-out bit, and the carry-in bit from the circuitry, add the separate propagate, kill, and generate bits of the third propagate, kill, and generate recoded number representation ~~in accordance~~ with ~~a~~ the carry-out bit and the carry-in bit to generate a sum value and a carry value.

2. (Original) The apparatus of claim 1, wherein said sum value and said carry value are dual rail encoded values.

3.–6. (Canceled)

7. (Currently Amended) A method for processing propagate, kill, and generate representations of respective first and second binary operands, comprising:

receiving a carry-in value and a first and a second propagate, kill, and generate representation of respective first and second binary operands;

adding the first and second propagate, kill, and generate representations to generate a third propagate, kill, and generate representation and a carry-out value; and

mathematically combining the third propagate, kill, and generate representation ~~in accordance~~ with the carry-out value and the carry-in value to generate a sum value and a carry value.

8. (Previously Presented) The method of claim 7, wherein said step of mathematically combining comprises adding the third propagate, kill, and generate representation and the carry-in value.

9. (Canceled)

10. (Previously Presented) The method of claim 7, wherein said step of mathematically combining further comprises generating dual rail encoded values.

11-22. (Canceled)